THE CHIP COMPLEXITY OF BINARY ARITHMETIC

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Abstract

The chip complexity of a computation is concerned with the chip area, A, and the time, T, required to perform the computation when implemented on a chip. An area-time product AT^{α}, for $\alpha \geq 0$, is used as a complexity measure. A particular value of α, which is chosen by the user, reflects the relative importance of A and T. We give both upper and lower bounds on the area-time complexity for chips that implement binary arithmetic, assuming a model of computation which is intended to approximate current and anticipated LSI or VLSI technology.

Comments

Only the Abstract is given here. The full paper appeared as [2]. The case $\alpha = 1$ was considered independently (using a more restrictive model than ours) by Abelson and Andreae [1]. Bounds for binary multiplication are also considered in [3], and the upper bound for binary addition is considered in more detail in [4]. For an extension of the lower bounds to problems with only a 1-bit output, see [5].

References

1. H. Abelson and P. Andreae, "Information transfer and area-time trade-offs for VLSI multiplication", *Communications of the ACM* 23 (1980), 20–23.
2. R. P. Brent and H. T. Kung, "The chip complexity of binary arithmetic" *Proc. Twelfth Annual ACM Symposium on the Theory of Computing*, ACM, New York, 1980, 190–200. rpb053.
3. R. P. Brent and H. T. Kung, "The area-time complexity of binary multiplication", *Journal of the ACM* 28 (1981), 521–534. CR 22#38242, MR 82i:68027. Corrigendum: *ibid* 29 (1982), 904. MR 83j:68046. rpb055.
4. R. P. Brent, and H. T. Kung, "A regular layout for parallel adders", *IEEE Transactions on Computers* C–31 (1982), 260–264. MR 83b:68002. rpb060.

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5. R. P. Brent and L. M. Goldschlager, "Some area-time tradeoffs for VLSI", *SIAM J. on Computing* 11 (1982), 737–747. MR 83k:68024. rpb064.

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