ON THE AREA OF BINARY TREE LAYOUTS

R. P. BRENT AND H. T. KUNG

Abstract

The binary tree is an important interconnection pattern for VLSI chip layouts. Suppose that the nodes are separated by at least unit distance and that a wire has unit width. The usual layout of a complete binary tree with n leaves takes chip area $\Omega(n \log n)$, but it can be arranged that all the leaves are on the boundary of the chip. In contrast, the "recursive H" layout has area of order n, but has only $O(\sqrt{n})$ leaves on the boundary. Thus, the recursive H layout enjoys a small area at the expense of a small number of possible I/O ports.

This note shows that it is not possible to design a complete binary tree layout with area $O(n)$ and all leaves on the boundary. More precisely, if the boundary of the chip is a convex plane curve and the leaves on the boundary are separated by at least unit distance, then area of order $n \log n$ is necessary just to accomodate all the wires.

Comments

Only the Abstract is given here. The full paper appeared as [2]. For related work, see [1, 3].

References

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