AN EFFICIENT ARCHITECTURE FOR SOLVING THE RECURSIVE CONVOLUTION EQUATION WITH HIGH THROUGHPUT

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Abstract

The one-dimensional (1D) recursive convolution problem plays a very important role in digital signal processing. It is usually considered that recursion implies sequential execution. Thus only 1D architectures were taken into account in VLSI implementation of this kind of problem. In this paper, we derive a two-dimensional systolic architecture for solving this problem with a throughput rate of two. Our solution has about twice the area, but twice the throughput of the previously known 1D systolic arrays. We also give an example to show that, by using our systolic architecture, IIR problems can be computed systolically with a throughput rate of two.

Comments

Only the Abstract is given here. The full paper appeared as [1]. For related work, see [2, 3, 4].

References

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1991 *Mathematics Subject Classification.* Primary 65Q05; Secondary 65G05.
Key words and phrases. Filter, IIR problem, recursive filter, recursive convolution equation, direct-form filter, stability, parallel algorithm, pipeline, systolic architecture, VLSI.

rpb099a typeset using $\mathcal{A}\mathcal{M}\mathcal{S}$-LaTeX