THE CHIP COMPLEXITY OF BINARY ARITHMETIC

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Abstract

The chip complexity of a computation is concerned with the chip area, A, and the time, T, required to perform the computation when implemented on a chip. An area-time product AT^α, for $\alpha \geq 0$, is used as a complexity measure. A particular value of α, which is chosen by the user, reflects the relative importance of A and T. We give both upper and lower bounds on the area-time complexity for chips that implement binary arithmetic, assuming a model of computation which is intended to approximate current and anticipated LSI or VLSI technology.

Comments

Only the Abstract is given here. The full paper appeared as [2]. The case $\alpha = 1$ was considered independently (using a more restrictive model than ours) by Abelson and Andreae [1]. Bounds for binary multiplication are also considered in [3], and the upper bound for binary addition is considered in more detail in [4]. For an extension of the lower bounds to problems with only a 1-bit output, see [5].

References

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