SOME AREA-TIME TRADEOFFS FOR VLSI

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Abstract

Area-time bounds on VLSI circuits for context-free language recognition, for the evaluation of propositional calculus formulae and for set equality and disjointness questions, are considered. In all cases, a lower bound $AT^{2\alpha} = \Omega(n^{1+\alpha})$ is proved, where A is the chip area, T the execution time, and $0 \leq \alpha \leq 1$. Similar results were known for computations with $\Omega(n)$-bit outputs, but the computations considered here have only 1-bit outputs. Upper bounds are also discussed.

Comments

Only the Abstract is given here. The full paper appeared as [2]. For related work on problems with $\Omega(n)$-bit outputs, see [1]. Upper bounds on the context-free language recognition problem are given in [3].

References

[1] R. P. Brent and H. T. Kung, "The area-time complexity of binary multiplication", *Journal of the ACM* 28 (1981), 521–534. CR 22#38242, MR 82i:68027. Corrigendum: *ibid* 29 (1982), 904. MR 83j:68046. rpb055.

[2] R. P. Brent and L. M. Goldschlager, "Some area-time tradeoffs for VLSI", *SIAM J. on Computing* 11 (1982), 737–747. MR 83k:68024. rpb064.

[3] R. P. Brent and L. M. Goldschlager, "A parallel algorithm for context-free parsing", *Proc. Seventh Australian Computer Science Conference*, special issue of *Australian Computer Science Communications* 6 (1984), 7.1–7.10. rpb085.

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