A REGULAR LAYOUT FOR PARALLEL ADDERS

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Abstract

With VLSI architectures, the chip area and design regularity represent a better measure of cost than the conventional gate count. We show that addition of n-bit binary numbers can be performed on a chip with a regular layout in time proportional to $\log n$.

Comments

Only the Abstract is given here. The full paper appeared as [1]. At the time of publication the use of carry-lookahead in VLSI designs was unpopular [3, Section 5.5], but more recently the Brent-Kung design technique has been applied widely in VLSI implementations of adders [4, Section 8.2.6]; also [2, A59–A61].

References

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